AMENDMENTS TO THE CLAIMS

1. (Withdrawn) A Simple Dynamic Differential Logic, comprising:

a differential logic cell having inverted inputs and corresponding non-inverted inputs, said differential logic cell configured to produce one or more inverted logic values and corresponding one or more non-inverted logic values; and

a pre-discharge stage, said one or more inverted logic values and said corresponding one or more non-inverted logic values provided to said pre-discharge stage, said pre-discharge stage providing one or more inverted outputs and one or more corresponding non-inverted outputs, said pre-discharge stage configured to provide an evaluation phase wherein the pre-discharge operator passes differential information, said pre-discharge stage further configured to provide a pre-discharge phase wherein said pre-discharge stage pre-discharges at least a portion of said differential logic cell.

2. (Withdrawn) A Simple Dynamic Differential Logic, comprising:

a differential logic cell having inverted inputs and corresponding non-inverted inputs, said differential logic cell configured to provide one or more inverted logic values and corresponding one or more non-inverted logic values; and

a pre-charge stage, said one or more inverted logic values and said corresponding one or more non-inverted logic values provided to said pre-charge stage, said pre-charge stage providing one or more inverted outputs and one or more corresponding non-inverted outputs, said precharge stage configured to provide an evaluation phase wherein the precharge operator passes differential information, said precharge stage further configured to provide a precharge phase wherein said precharge stage precharges at least a portion of said differential logic cell.

3. (Currently Amended) A Wave Dynamic Differential Logic, comprising:

a differential logic cell having inverted inputs and corresponding non-inverted inputs, said differential logic cell configured to provide one or more inverted logic outputs and corresponding one or more non-inverted logic outputs, said differential logic cell configured to receive a precharge wave and/or a predischarge wave on said inverted inputs and non-inverted inputs and to propagate [[a]] said precharge wave and/or ~~a predischarges~~ said predischarge wave from said inverted inputs and corresponding non-inverting inputs to said inverted logic outputs and said non-inverted logic outputs.

4. (Currently Amended) A Wave Dynamic Differential Logic, comprising:

a differential logic cell having inverted inputs and corresponding non-inverted inputs, said differential logic cell configured to provide one or more inverted logic outputs and corresponding one or more non-inverted logic outputs; and

a pre-discharged logic cell configured to receive a pre-discharge signal and, in response to said pre-discharge signal, to generate a pre-discharge wave to pre-discharge and propagate through said differential logic cell from said inverted inputs and non-inverted inputs to said inverted logic outputs and non-inverted logic outputs and/or a precharged logic cell configured to receive a precharge signal and, in response to said precharge signal, to generate a precharge wave to pre-charge and propagate through said differential logic cell from said inverted inputs and non-inverted inputs to said inverted logic outputs and non-inverted logic outputs.

5. (Currently Amended) A Wave Dynamic Differential Logic, comprising:

a differential logic cell having inverted inputs and corresponding non-inverted inputs, said differential logic cell configured to provide one or more

inverted logic outputs and corresponding one or more non-inverted logic outputs; and

a master-slave differential dynamic logic register configured to receive a precharge signal and, in response to said precharge signal, to generate a pre-charge wave to pre-charge and propagate through said differential logic cell from said inverted inputs and non-inverted inputs to said inverted logic outputs and non-inverted logic outputs.

6. (Currently Amended) A Wave Dynamic Differential Logic, comprising:

a differential logic cell having inverted inputs and corresponding non-inverted inputs, said differential logic cell configured to provide one or more inverted logic outputs and corresponding one or more non-inverted logic outputs; and

a master-slave differential dynamic logic register configured to receive a pre-discharge signal and, in response to said pre-discharge signal, to generate a pre-discharge wave in response to said pre-discharge signal to pre-discharge and propagate through said differential logic cell from said inverted inputs and non-inverted inputs to said inverted logic outputs and non-inverted logic outputs.

7. (Currently Amended) A Divided Wave Dynamic Differential Logic DPA-resistant logic circuit, comprising:

a first logic tree comprising a plurality of first logic tree inputs and a plurality of first logic tree outputs and configured to, during an evaluation phase, receive inverted ~~inputs~~ input data and corresponding non-inverted ~~inputs~~ input data on said first logic tree inputs and to produce ~~one or more~~ first ~~outputs~~ output data on said first logic tree outputs; and

a dual of said first logic tree comprising a plurality of dual logic tree inputs and a plurality of dual logic tree outputs and configured to, during said evaluation phase, receive said inverted ~~inputs~~ input data and said corresponding

non-inverted ~~inputs~~ input data on said dual logic tree inputs and produce ~~one or more~~ inverted first ~~outputs~~ output data on said dual logic tree outputs,

said first logic tree and said dual of said first logic tree further configured to, during a precharge and/or pre-discharge phase, receive a precharge wave and/or a pre-discharge wave on said first logic tree inputs and said dual logic tree inputs and propagate said precharge wave and/or pre-discharge wave to said first logic tree outputs and said dual logic tree outputs.

8. (Cancelled)

9. (Currently Amended) A Wave Dynamic Differential Logic, comprising:

a differential logic cell having inverted inputs and corresponding non-inverted inputs, said differential logic cell configured to provide one or more inverted logic outputs and corresponding one or more non-inverted logic outputs; and

a master-slave differential dynamic logic register configured to receive a pre-charge wave and to transmits on [[a]] the pre-charge wave to pre-charge said differential logic cell, the differential logic cell further configured to receive the precharge wave on said inverted inputs and non-inverted inputs and to propagate said pre-charge wave from said inverted inputs and corresponding non-inverting inputs to said inverted logic outputs and said non-inverted logic outputs.

10. (Currently Amended) A Wave Dynamic Differential Logic, comprising:

a differential logic cell having inverted inputs and corresponding non-inverted inputs, said differential logic cell configured to provide one or more inverted logic outputs and corresponding one or more non-inverted logic outputs; and

a differential dynamic logic register configured to receive a pre-charge signal and, in response to said pre-charge signal, to generate a pre-charge wave to pre-charge said differential logic cell, the differential logic cell further configured to receive the precharge wave on said inverted inputs and non-inverted inputs and to propagate said pre-charge wave from said inverted inputs and corresponding non-inverting inputs to said inverted logic outputs and said non-inverted logic outputs.

11. (Currently Amended) A Wave Dynamic Differential Logic, comprising:

a differential logic cell having inverted inputs and corresponding non-inverted inputs, said differential logic cell configured to provide one or more inverted logic outputs and corresponding one or more non-inverted logic outputs; and

a master-slave differential dynamic logic register configured to receive a pre-discharge wave and to transmits on [[a]] the pre-discharge wave to pre-discharge said differential logic cell, the differential logic cell further configured to receive the pre-discharge wave on said inverted inputs and non-inverted inputs and to propagate said pre-discharge wave from said inverted inputs and corresponding non-inverting inputs to said inverted logic outputs and said non-inverted logic outputs.

12. (Currently Amended) A Wave Dynamic Differential Logic, comprising:

a differential logic cell having inverted inputs and corresponding non-inverted inputs, said differential logic cell configured to provide one or more inverted logic outputs and corresponding one or more non-inverted logic outputs; and

a differential dynamic logic register configured to receive a pre-discharge signal and generate a pre-discharge wave to pre-discharge said differential logic cell, the differential logic cell further configured to receive the pre-discharge wave

on said inverted inputs and non-inverted inputs and to propagate said pre-discharge wave from said inverted inputs and corresponding non-inverting inputs to said inverted logic outputs and said non-inverted logic outputs.

13. (Withdrawn) A method for differential pair conductor routing in a logic circuit, comprising:

routing conductors to obtain vertical conductors, horizontal conductors, and vias to connect said vertical conductors and said horizontal conductors;

transforming at least one of said vertical conductors into parallel first and second differential vertical conductors;

transforming at least one of said horizontal conductors into parallel first and second differential horizontal conductors; and

transforming a via connecting said at least one of said vertical conductors to said at least one of said horizontal conductors into first and second vias; said first via connecting said first differential vertical conductor to said first differential horizontal conductor and said second via connecting said second differential vertical conductor to said second differential horizontal conductor.

14. (Withdrawn) A method for differential pair conductor routing in a logic circuit, comprising:

routing conductors of a first line width to obtain vertical conductors of said first line width, horizontal conductors of said first line width, and vias to connect said vertical conductors and said horizontal conductors;

separating at least one of said vertical conductors of said first line width into parallel first and second differential vertical conductors of a second line width;

separating at least one of said horizontal conductors of said first line width into parallel first and second differential horizontal conductors of said second line width;

separating a via connecting said at least one of said vertical conductors to said at least one of said horizontal conductors into first and second vias; said

first via connecting said first differential vertical conductor to said first differential horizontal conductor and said second vial connecting said second differential vertical conductor to said second differential horizontal conductor.

15. (Withdrawn) The method of Claim 13 or 14, further comprising replacing conventional logic used for said routing with differential logic.

16. (Withdrawn) The method of Claim 14, wherein said second line width is smaller than one-half of said first line width

17. (Withdrawn) The method of Claim 13 or 14, wherein a centerline of a space between said parallel first and second differential horizontal conductors corresponds to a centerline of said at least one horizontal conductor.

18. (Withdrawn) The method of Claim 13 or 14, wherein a centerline of a space between said parallel first and second differential vertical conductors corresponds to a centerline of said at least one vertical conductor.

19. (Withdrawn) A method for differential pair conductor routing in a logic circuit, comprising:

routing conductors of a first line width to obtain a first routing for a first logic library, wherein vertical and horizontal paths are separated such that vertical and horizontal conductors do not short, wherein connections between said vertical and horizontal paths are provided by vias;

separating conductor paths in said first routing into differential paths by splitting said conductors of a first line width into spaced parallel conductors of a second line width, where said second line width is smaller than said first line width;

separating said vias into pairs of vias; and

replacing said first logic library with a differential logic library.

20. (Withdrawn) A method for differential pair conductor routing in a logic circuit, comprising:

routing conductors of a first line width to obtain a first routing for a first logic library, wherein vertical and horizontal paths are separated such that vertical and horizontal conductors do not short, wherein connections between said vertical and horizontal paths are provided by vias;

separating conductor paths in said first routing into differential paths by splitting said conductors of a first line width into spaced parallel conductors of a second line width;

separating said vias into pairs of vias; and

replacing said first logic library with a differential logic library.

21. (Withdrawn) The method of claim 21, wherein parasitic capacitance is reduced by disposing a conductor between one or more differential pairs.

22. (Withdrawn) The method of claim 21, wherein parasitic capacitance is reduced by increasing a distance between one or more differential pairs.

23. (Original) The Wave Dynamic Differential Logic of Claim 3, comprising positive logic.

24. (Original) The Wave Dynamic Differential Logic of Claim 4, comprising positive logic.

25. (Original) The Wave Dynamic Differential Logic of Claim 5, comprising positive logic.

26. (Original) The Wave Dynamic Differential Logic of Claim 6, comprising positive logic.

27. (New) The Wave Dynamic Differential Logic of Claim 3, wherein said differential logic cell receives and propagates said precharge wave and/or said predischarge wave during a precharge and/or pre-discharge phase, and is further configured to, during an evaluation phase, receive differential data on said inverted inputs and said corresponding non-inverted inputs and evaluate said differential data to produce differential output data on said inverted logic outputs and said non-inverted logic outputs.